AK4524

24-Bit 96kHz Audio CODEC

Features

- 24-bit Stereo Digital-to-Analog Converter (DAC)
  - Dynamic range and S/R: 110dB
  - S/(N + D): 94dB
  - 128x oversampling
  - 24-bit 8x interpolation filter
  - Differential outputs
- 24-bit Stereo Analog-to-Digital Converter (ADC)
  - Dynamic range and S/R: 100dB
  - S/(N + D): 90dB
  - Digital HPF for offset cancellation
- High jitter tolerance
- 3-wire serial output interface
- Master mode and slave mode
- 5V operation
- 3V power supply pin for 3V interface
- Small 28-pin VSOP package

Description

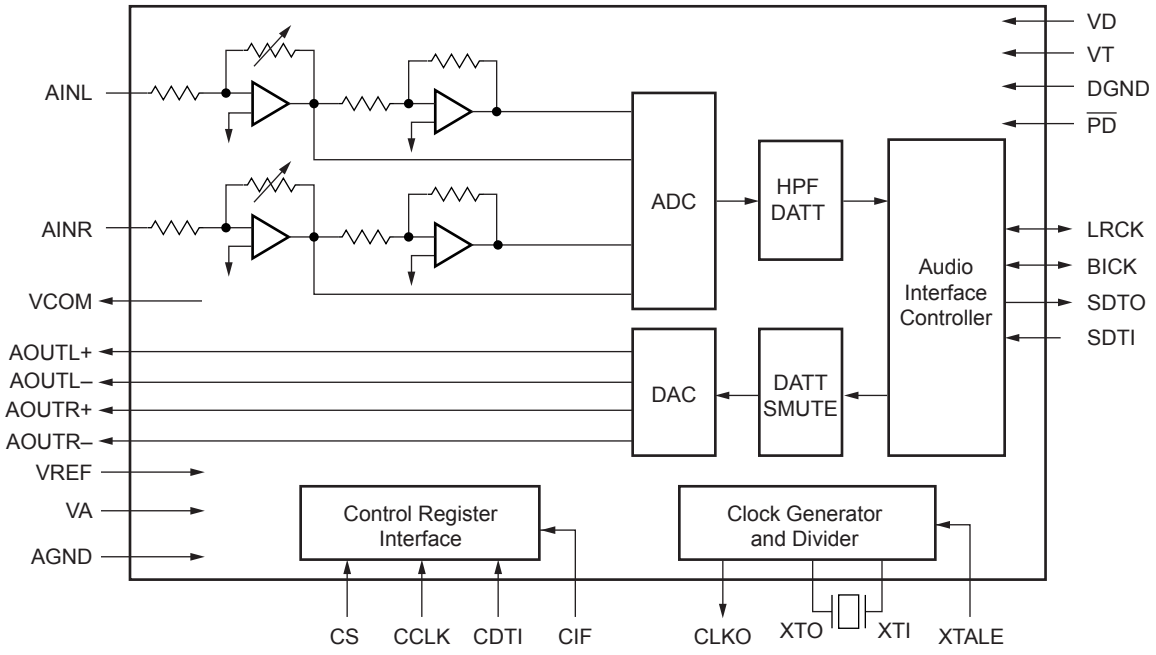
The AK4524 is a high-performance 96kHz, 24-bit, stereo CODEC. Its superior performance is achieved through innovative technologies and high integration, making this part ideal for musical instruments, MD players, and other demanding applications.

The DAC in the AK4524 uses AKM's multi-bit architecture to achieve 110dB Dynamic Range (DR) and Signal-to-Noise Ratio (SNR). In addition, the DAC offers full differential outputs, switched capacitor filtering, output digital attenuation, soft mute, and outstanding clock jitter tolerance.

The ADC takes advantage of AKM's dual-bit architecture to achieve 100dB of DR and SNR, and 96kHz sampling rate capability. Its integrated Programmable Gain Amplifier (PGA) facilitates the design of recording equipment with outstanding DR.

The AK4524 is packaged in a small 28-pin VSOP package that minimizes board space usage.

Block Diagram



Performance Specifications

Analog Characteristics

Ta = 25°C, VREF = VA = VD = VT = 5.0V, AGND = DGND = 0V, fs = 44.1kHz, Signal Frequency = 1kHz, 24-bit data, Measurement frequency = 10Hz to 20kHz at fs = 44.1kHz or 10Hz to 40kHz at fs = 96kHz, IPGA at 0dB gain, unless otherwise specified.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
ADC Analog Input Characteristics					
Resolution				24	Bits
Dynamic Range[1]	fs = 44.1kHz, A-weighted	94	100		dB
	fs = 96kHz	88	96		
Signal-to-Noise Ratio	fs = 44.1kHz, A-weighted	94	100		dB
	fs = 96kHz	88	96		
Signal-to-(Noise + Distortion) Ratio[2]	fs = 44.1kHz	84	90		dB
	fs = 96kHz	80	88		
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20		ppm/°C
Power Supply Rejection[3]			50		dB
DAC Analog Output Characteristics					
Resolution				24	Bits
Dynamic Range[1]	fs = 44.1kHz, A-weighted	104	110		dB
	fs = 96kHz	96	104		
Signal-to-Noise Ratio	fs = 44.1kHz, A-weighted	104	110		dB
	fs = 96kHz	96	104		
Signal-to-(Noise + Distortion) Ratio	fs = 44.1kHz	88	94		dB
	fs = 96kHz	85	93		
Interchannnel Isolation		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20		ppm/°C
Output Voltage[4]	(AOUT+) - (AOUT-)	5.0	5.4	5.8	V_{p-p}
Load Resistance	AC load	5			kΩ
Output Current	AC load			1.5	mA
Load Capacitance				25	pF
Power Supply Rejection[3]			50		dB
Input PGA Characteristics					
Input Voltage		2.7	2.9	3.1	Vp-p
Input Resistance		5	10	15	kΩ
Step Size		0.2	0.5	0.8	dB
Gain Control Range		0		18	dB

Performance Specifications (Continued)

Analog Characteristics (Continued)

Ta = 25°C, VREF = VA = VD = VT = 5.0V, AGND = DGND = 0V, fs = 44.1kHz, Signal Frequency = 1kHz, 24-bit data, Measurement frequency = 10Hz to 20kHz at fs = 44.1kHz or 10Hz to 40kHz at fs = 96kHz, IPGA at 0dB gain, unless otherwise specified.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Power Supplies					
Normal Operation, (PD = H)	VA		30	45	mA
	VD + VT for fs = 44.1kHz		16	24	
	VD + VT for fs = 96kHz		24	36	
Power-down Mode, (PD = L)	VA		10	100	µA
	VD + VT		10	100	µA

Digital Characteristics

Ta = 25°C, VA = VD = 4.75V to 5.25V, VT = 2.7V to 5.25V.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Input					
High-Level Input Voltage (VIH)		2.2			V
Low-Level Input Voltage (VIL)				0.8	V
Input Leakage Current				±10	µA
Output					
High-Level Output Voltage[5] (VOH)	Iout = -100µA	2.7/VT-0.5			V
Low-Level Output Voltage (VOL)	Iout = 100µA			0.5	V

Filter Characteristics

Ta = 25°C, VA = VD = 4.75V to 5.25V, VT = 2.7V to 5.25V, fs = 44.1kHz, DEM off.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
ADC Digital Low Pass Filter					
Passband[6]	-0.005dB	0		19.76	kHz
	-0.02dB		20.02		
	-0.06dB		20.20		
	-6.0dB		22.05		
Stopband		24.34			kHz
Passband Ripple				±0.005	dB
Stopband Attenuation		80			dB
Group Delay[7]			31		1/fs
Group Delay Distortion			0		µs
ADC Digital High Pass Filter					
Frequency Response[6]	-3dB		0.9		Hz
	-0.5dB		2.7		
	-0.1dB		6.0		

Performance Specifications (Continued)

Filter Characteristics (Continued)

Ta = 25°C, VA = VD = 4.75V to 5.25V, VT = 2.7V to 5.25V, fs = 44.1kHz, DEM off.

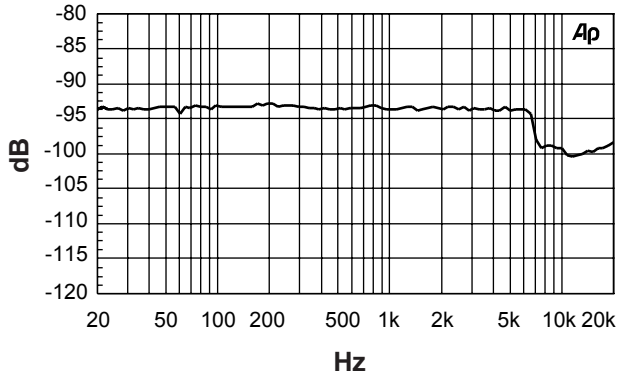
Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
DAC Digital Filter					
Passband[6]	-0.06dB	0		20.0	kHz
	-6.0dB		22.05		
Stopband		24.1			kHz
Passband Ripple				±0.005	dB
Stopband Attenuation		75			dB
Group Delay[7]			30		1/fs
DAC Digital Filter + SCF					
Frequency Response	0 to 20.0kHz		±0.2		dB
	to 40.0kHz (for fs = 96kHz)		±0.3		

Notes:

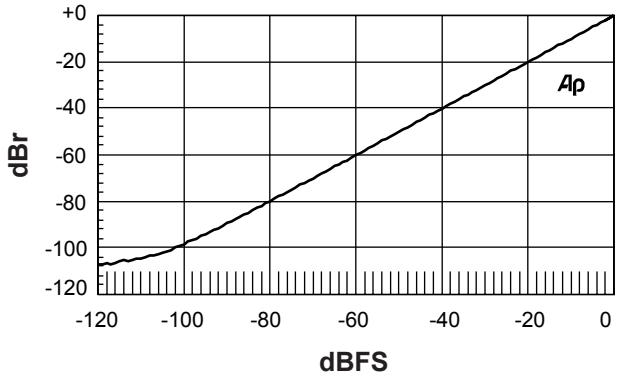
1. Dynamic Range measured at -60dBFS.
2. Signal-to-(Noise + Distortion) Ratio measured at -0.5dBFS.
3. PSR is applied to VA, VD, and VT with 1kHz, 50mV$_{p-p}$. The VREF pin is held at a constant voltage.
4. This voltage is proportional to VREF: Output Voltage = 1.08 x VREF x Gain.
5. The minimum value is the lower voltage of 2.7V or VT - 0.5V.
6. The passband and stopband frequencies scale with fs. For example, 20.02kHz (-0.02dB) is 0.454 x fs. The reference frequency of these responses is 1kHz.
7. Group delay (GD) is the delay time which occurs in the digital filter. On the ADC, this delay is measured from the start of the analog input to the start of the digital output. On the DAC, GD is measured from the time when the DAC begins receiving data, to the time when the analog data begins to be output.

Typical Performance Curves

DAC: THD + N vs. Frequency

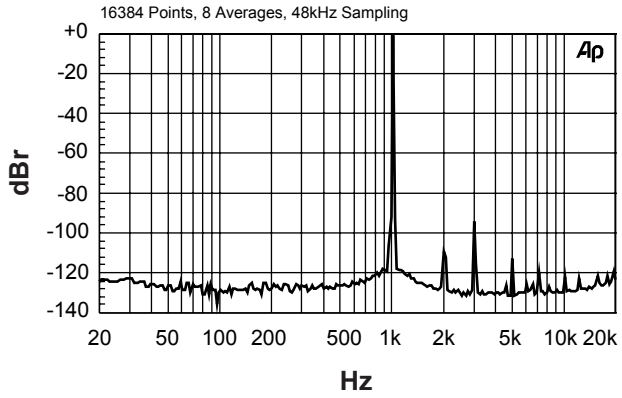


DAC: Linearity

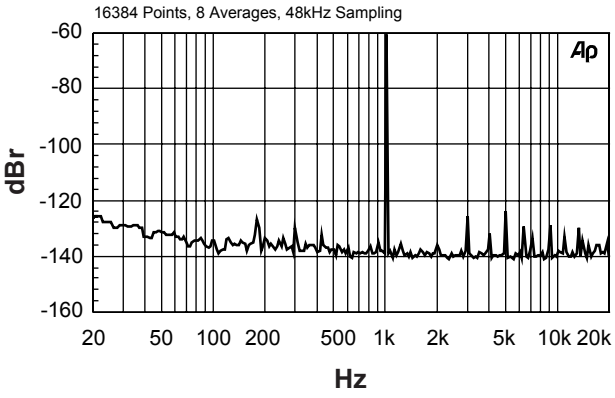


Typical Performance Curves (Continued)

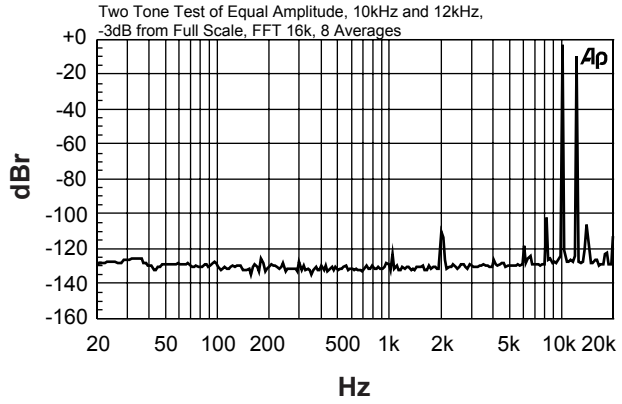
DAC: 0dB FFT



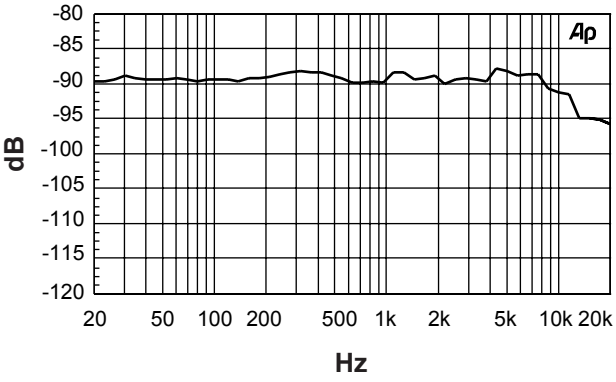
DAC: -60dB FFT



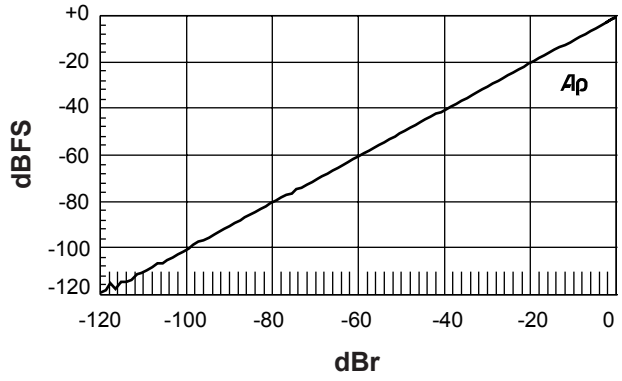
DAC: Two Tone



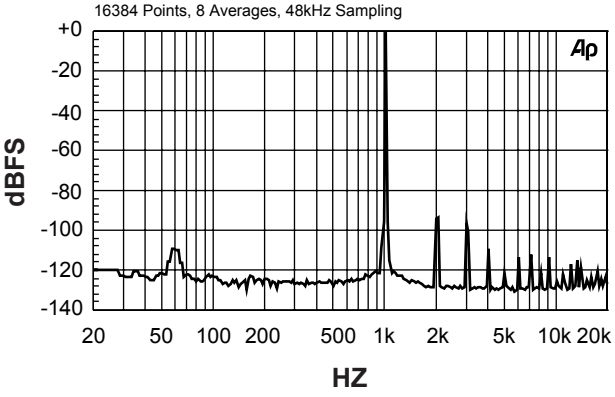
ADC: THD + N vs. Frequency



ADC: Linearity

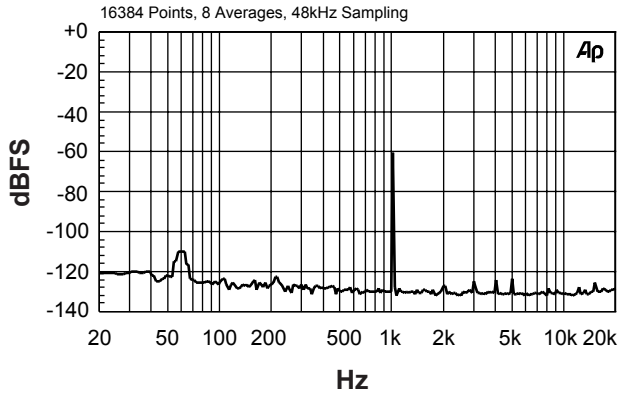


ADC: 0dB FFT

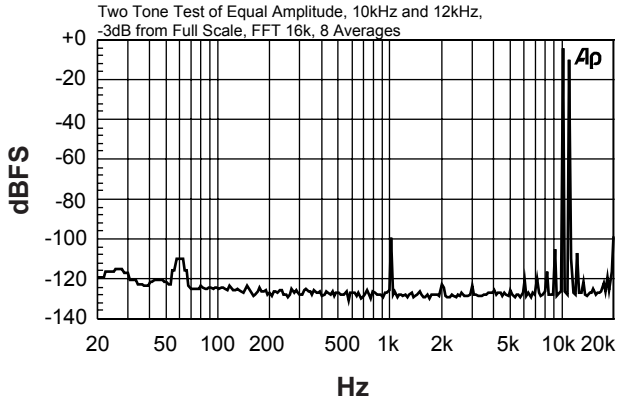


Typical Performance Curves (Continued)

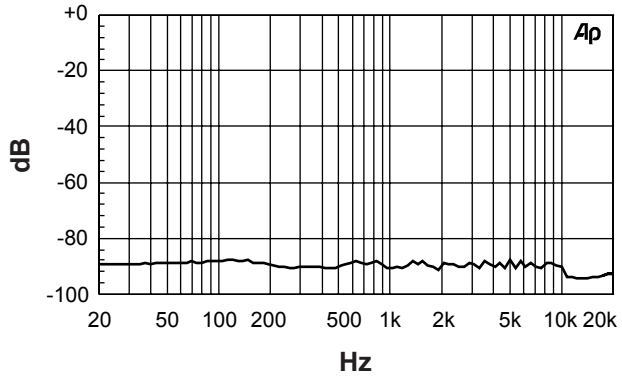
ADC: -60dB FFT



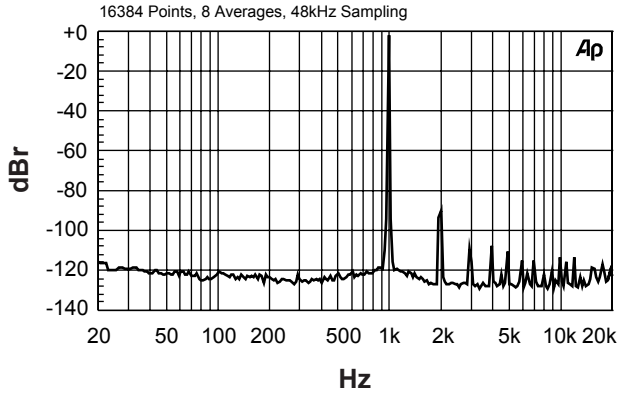
ADC: Two Tone



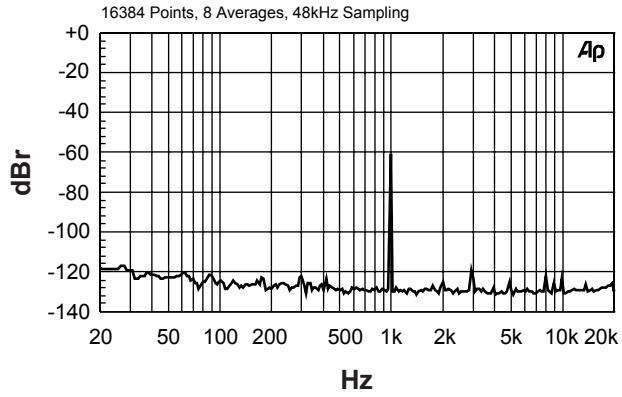
AD-to-DA: THD + N vs. Frequency



AD-to-DA: 0dB FFT



AD-to-DA: -60dB FFT



Absolute Maximum Ratings

AGND and DGND = 0V. All voltages are with respect to ground.

Parameter	Min.	Max.	Units
Power Supplies			
Analog, VA	-0.3	6.0	V
Digital, VD	-0.3	6.0	V
Output Buffer, VT	-0.3	6.0	V
VD - VA		0.3	V
Input Current—Any Pin Except Power Supplies	-	± 10	mA
Analog Input Voltage	-0.3	VA + 0.3	V
Digital Input Voltage	-0.3	VA + 0.3	V
Temperature			
Ambient Operating Temperature (Power Applied)	-10	70	°C
Storage Temperature	-65	150	°C

Caution:
Exceeding minimum and maximum ratings may result in damage to the device.

Recommended Operating Conditions

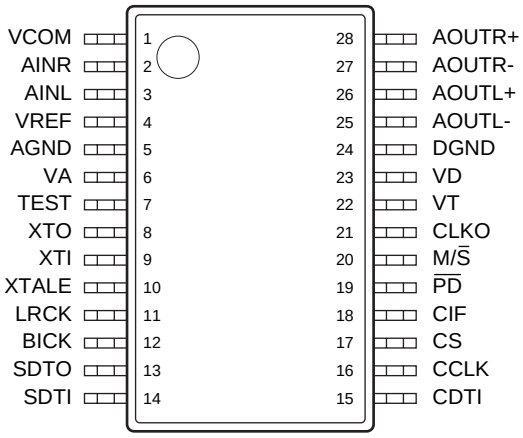
AGND and DGND = 0V. All voltages are with respect to ground.

Parameter	Min.	Typ.	Max.	Units
Power Supplies[1]				
Analog, VA	4.75	5.0	5.25	V
Digital, VD	4.75	5.0	VA	V
Output Buffer, VT	2.7	3.0	VD	V
References				
Voltage Reference, VREF	3.0		VA	V

Note:

1. VA and VD should be powered at the same time or VA should be powered earlier than VD. The power-up sequence between VA and VT, or between VD and VT is not critical.

Pin Layout



Pin Descriptions

No.	Pin Name	I/O	Pin Function and Description
1	VCOM	O	**Common Voltage Output.** VCOM = VA/2.
2	AINR	I	**Right Analog Input.**
3	AINL	I	**Left Analog Input.**
4	VREF	I	**Voltage Reference Input Pin.** VREF = VA normally. The ADC and DAC use this pin as a voltage reference. This pin is normally connected to VA through an external filter.
5	AGND	-	**Analog Ground.**
6	VA	-	**Analog Power Supply.** 5V normally.
7	TEST	I	**Test Pin.** Do not connect (internal pull-down pin).
8	XTO	O	**Crystal Output.**
9	XTI	I	**Crystal or Master Clock Input.**
10	XTALE	I	**Crystal Oscillator Enable.** When High, the oscillator is enabled. When Low, the oscillator is disabled.
11	LRCK	I/O	**Input/Output Channel Clock.** Defines the sampling rate, fs.
12	BICK	I/O	**Audio Serial Data Clock.** A clock input of 32fs or more is recommended.
13	SDTO	O	**Audio Serial Data Output.**
14	SDTI	I	**Audio Serial Data Input.**
15	CDTI	I	**Control Data Input.** This pin is for the serial control input, see Table XX.
16	CCLK	I	**Control Data Clock.**
17	CS	I	**Chip Select.** For use in writing serial control data.
18	CIF	I	**Control Data Interface Format.** When this pin is High, the CS input signal triggers on the falling edge. When Low, CS triggers on the rising edge.
19	PD	I	**Power-down Mode.** When PD is High, the chip powers up. When Low, the chip is in powerdown mode.
20	M/S	I	**Master/Slave Mode Select.** When High, the device is in Master mode. When Low, it is in Slave mode.
21	CLKO	O	**Master Clock Output.**

Pin Descriptions (Continued)

No.	Pin Name	I/O	Pin Function and Description
22	VT	-	**Output Buffer Power Supply.** VT = 5V or 3.3V normally.
23	VD	-	**Digital Power Supply.** 5V normally.
24	DGND	-	**Digital Ground.**
25	AOUTL-	O	**Left Channel Negative Analog Output.**
26	AOUTL+	O	**Left Channel Positive Analog Output.**
27	AOUTR-	O	**Right Channel Negative Analog Output**.
28	AOUTR+	O	**Right Channel Positive Analog Output.**

Note:

1. All input pins, except the TEST pin, should be connected.

Swithching Characteristics

Ta = 25°C, VA and VD = 4.75V to 5.25V, VT = 2.7V to 5.25V, C_L = 20pF.

Parameter		Conditions/Comments	Min.	Typ.	Max.	Units
Master Clock Timing						
Crystal Resonator Frequency			11.2896		24.576	MHz
fCLK	External Clock Frequency		8.192		49.152	MHz
tCLKL	External Clock Pulse Width Low		0.4/fCLK			ns
tCLKH	External Clock Pulse Width High		0.4/fCLK			ns
CLKO Output—Crystal Mode						
fMCK	Frequency		11.2896		24.576	MHz
dMCK	Duty Cycle		35	50	65	%
LRCK Frequency						
fsn	Normal Speed Mode	DFS0 = 0, DFS1 = 0	32		48	kHz
fsd	Double Speed Mode	DFS0 = 1, DFS1 = 0	64		96	kHz
fsq	Quad Speed Mode	DFS0 = 0, DFS1 = 1 See Note 1	128		192	kHz
Duty Cycle	Slave Mode		45		55	%
	Master Mode			50		%
Audio Interface Timing—Slave Mode						
tBCK	BICK Period		81			ns
tBCKL	BICK Pulse Width Low		33			ns
tBCKH	BICK Pulse Width High		33			ns
tLRB	LRCK Edge to Rising edge of BICK	See Note 2	20			ns
tBLR	Rising Edge of BICK to LRCK Edge	See Note 2	20			ns
tLRS	LRCK to SDTO (MSB)	Except in IIS Mode			40	ns
tBSD	Falling Edge of BICK to SDTO				40	ns
tSDH	SDTI Hold Time		20			ns
tSDS	SDTI Setup Time		20			ns

Switching Characteristics (Continued)

Ta = 25˚C, VA and VD = 4.75V to 5.25V, VT = 2.7V to 5.25V, C_L = 20pF.

Parameter		Conditions/Comments	Min.	Typ.	Max.	Units
Audio Interface—Master Mode						
fBCK	BICK Frequency			64fs		Hz
dBCK	BICK Duty Cycle			50		%
tMBLR	Falling Edge of BICK to LRCK		-20		20	ns
tBSD	Falling Edge of BICK to SDTO		-20		20	ns
tSDH	SDTI Hold Time		20			ns
tSDS	SDTI Setup Time		20			ns
Control Interface Timing—CIF = 0						
tCCK	CCLK Period		200			ns
tCCKL	CCLK Pulse Width Low		80			ns
tCCKH	CCLK Pulse Width High		80			ns
tCDS	CDTI Setup Time		40			ns
tCDH	CDTI Hold Time		40			ns
tCSW	CS High Time		150			ns
tCSW	CS Low Time		150			ns
tCSS	Rising Edge of CS to Rising Edge of CCLK		150			ns
tCSH	Rising Edge of CCLK to Rising Edge of CS		50			ns
Control Interface Timing—CIF = 1						
tCCK	CCLK Period		200			ns
tCCKL	CCLK Pulse Width Low		80			ns
tCCKH	CCLK Pulse Width High		80			ns
tCDS	CDTI Setup Time		40			ns
tCDH	CDTI Hold Time		40			ns
tCSW	CS High Time		150			ns
tCSW	CS Low Time		150			ns
tCSS	Falling Edge of CS to Rising Edge of CCLK		150			ns
tCSH	Rising Edge of CCLK to Falling Edge of CS		50			ns
Reset Timing						
tPD	$\overline{PD}$ Pulse Width	See Note 3	150			ns
tPDV	Rising Edge of RSTAD to Valid SDTO	See Note 4		516		1/fs

Notes:

1. The AK4524 ADC is disabled in this mode.
2. BICK Rising edge must not occur at the same time as the LRCK edge.
3. The AK4524 can be reset by bringing $\overline{PD}$ Low.
4. These cycles are the number of LRCK pulses rising from the RSTAD bit. Refer to the Register Map and Control Register Definitions sections for additional information.

Timing Diagrams

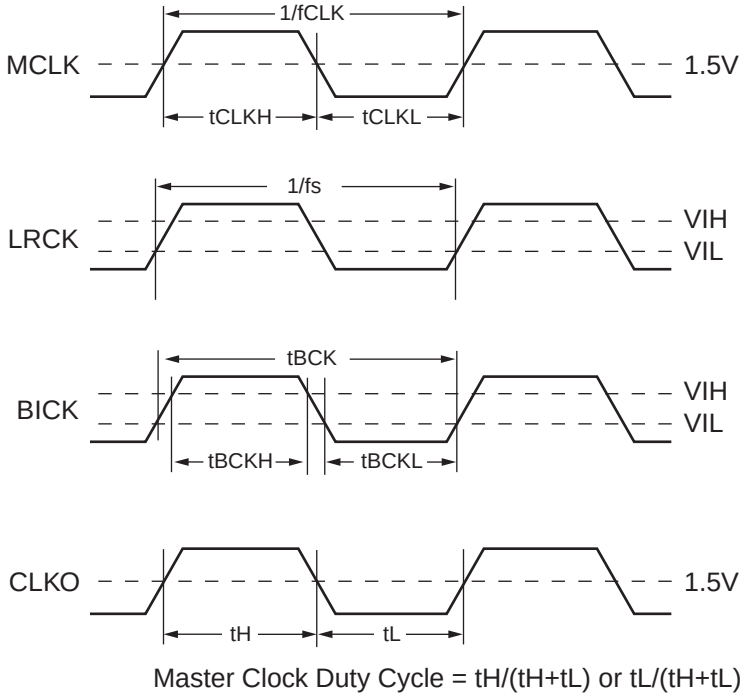


Figure 1. Clock Timing

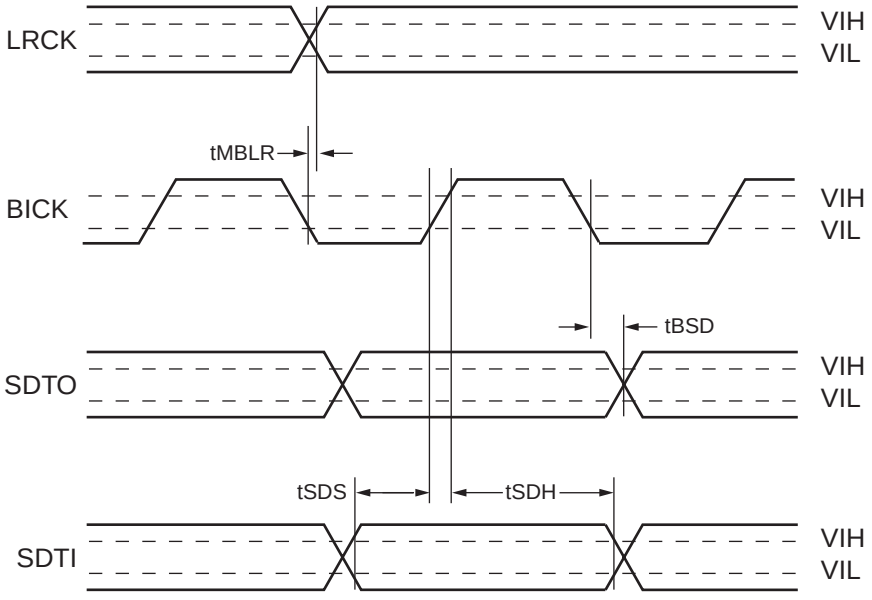


Figure 2. Audio Interface in Master Mode

Timing Diagrams (Continued)

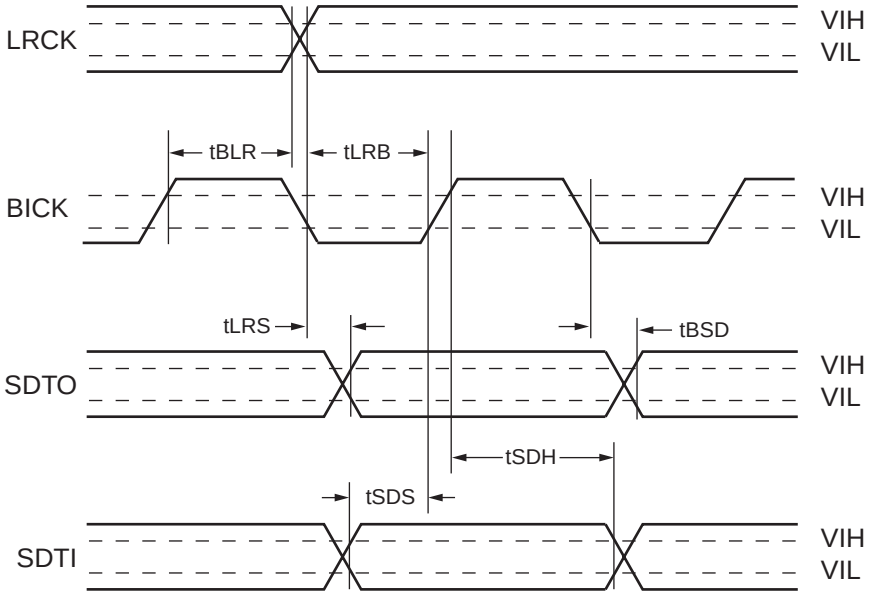


Figure 3. Audio Interface in Slave Mode

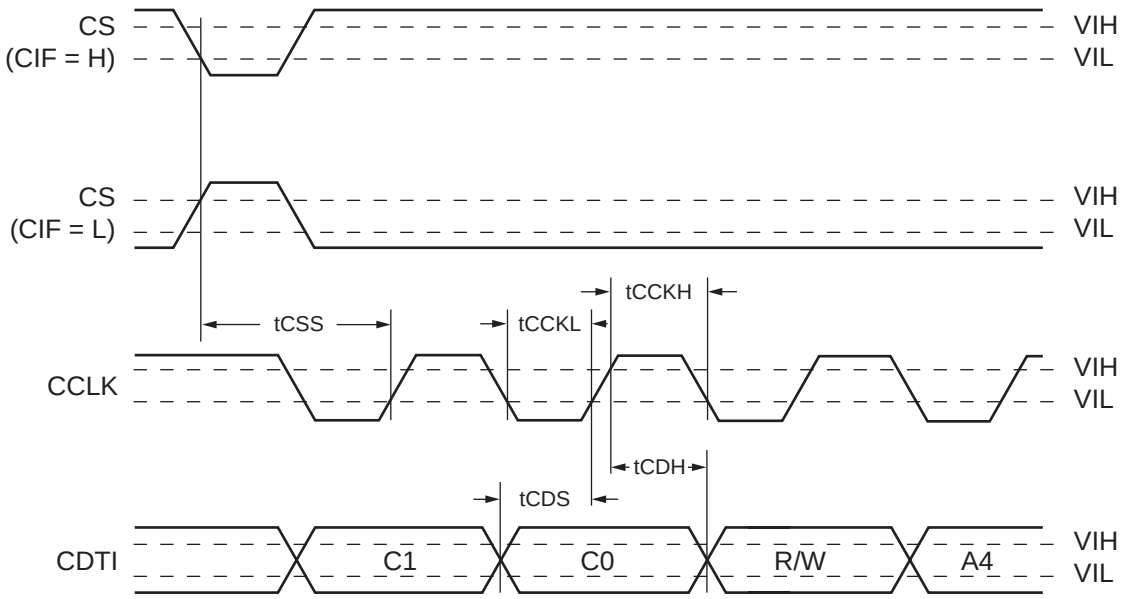


Figure 4. WRITE Command Input Timing

Timing Diagrams (Continued)

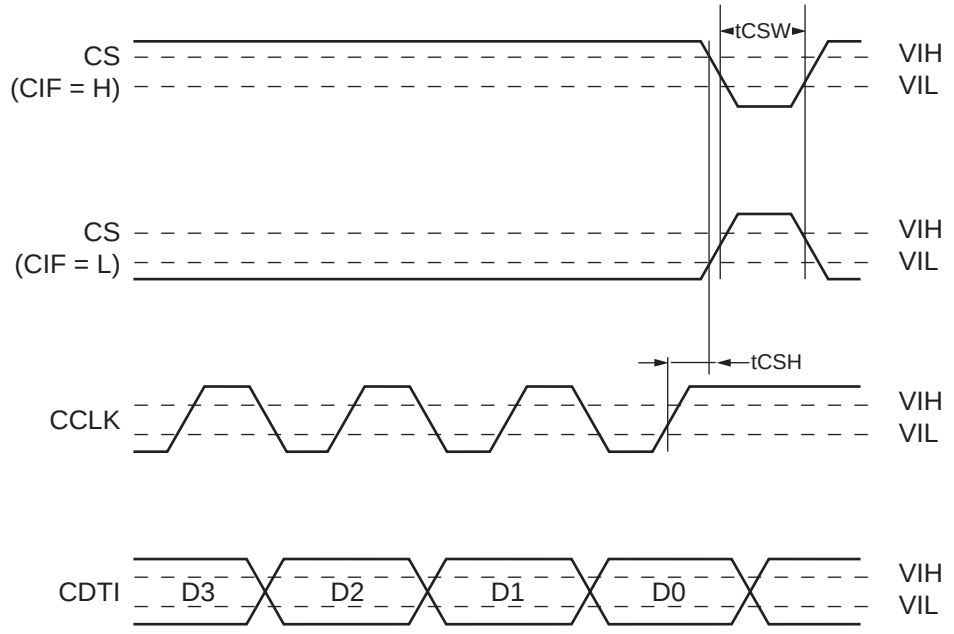


Figure 5. Write Data Input Timing

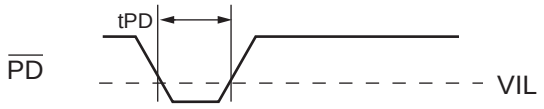


Figure 6. Power-Down and Reset Timing

Device Operation

System Clock Input

The master clock (MCLK) can be either a crystal oscillator placed across the XTI and XTO pins, or an external clock that is input at the XTI pin leaving the XTO pin floating. The master clock frequency can be selected using the CMODE, CKS0, and CKS1 control registers (see Table 1). The sampling speed is selected using the DFS0 and DFS1 registers, and can be set to normal mode, double mode, and four-times (quad) speed monitor mode (see Table 2). When the device runs in the quad mode, the ADC remains powered down and inactive. The frequency of the master clock output (CKLO) is the same as the MCLK frequency, and the output can be enabled or disabled using the XTALE pin.

When using a crystal oscillator, external loading capacitors are required between the XTI and XTO pins, and DGND.

In the slave mode, the LRCK clock input must be synchronized with the master clock, MCLK, but the phase is not critical. Internal timing is synchronized at power-up. All external clocks must be present unless $\overline{PD}$ is Low, or unless all sections are powered down using the control registers. Otherwise, excessive current may flow due to the internal dynamic logic. In the master mode, the clocks can be supplied from a crystal oscillator or from an external clock. If using a crytal oscillator, the clock's output remains active during power-down. If an external clock is used, then it should not be stopped even during power-down.

> **Caution:**
> Due to its internal dynamic refresh logic, prolonged periods of time without external clock input may result in damage to the device.

Table 1. Master Clock Frequency Select

CMODE	CKS1	CKS0	MCLK
0	0	0	256fsn[1]
0	0	1	512fsn
0	1	0	1024fsn
1	0	0	384fsn
1	0	1	768fsn

Notes:
1. Power-up and reset default.
2. fsn is the sampling rate in the normal speed mode.

Table 2. Sampling Speed

DFS1	DFS0	Sampling Rate		Monitor Mode
0	0	fsn	Normal Speed (Reset Default)	
0	1	fsd = 2 x fsn	Double Speed	
1	0	fsq = 4 x fsn	4 Times Speed[1] (SDTO = L)	Simple Decimation
1	1	fsq = 4 x fsn	4 Times Speed[1] (SDTO = L)	2 Tap Filter

Note:
1. The ADC is powered down in this mode.

Table 3. Master Clock Frequency

Master Clock			Normal Speed Mode	Double Speed Mode	Quad Speed Mode
MCLK	fsn = 44.1kHz	fsn = 48kHz			
256fsn	11.2896MHz	12.288MHz	256fns	N/A	N/A
512fsn	22.5792MHz	24.576MHz	512fsn	256fsd	128fsq
1024fsn	45.1584MHz	49.152MHz	1024fsn	512fsd	256fsq
384fsn	16.9344MHz	18.432MHz	384fsn	N/A	N/A
768fsn	33.8688MHz	36.864MHz	768fsn	384fsd	192fsq

Note:
1. Crystals from 11.2892MHz to 24.576MHz can be used. Frequencies higher than 24.576MHz are supported only when using an external clock.

Audio Serial Interface Format

The AK4524 supports five serial data modes that can be selected using the DIF0, DIF1, and DIF2 register bits as shown in Table 4. The serial data input for these modes is MSB-first and 2's complement. The SDTO is clocked on the falling edge of BICK and the SDTI signal is latched to the rising edge of BICK.

This interface supports both master mode and slave mode. In the master mode, BICK and LRCK are outputs and the frequency of BICK is fixed to 64fs. Figures 7 through 11 show the timing diagrams for the different modes.

Table 4. Audio Data Format

Mode	DIF2	DIF1	DIF0	Serial Data Output SDTO	Serial Data Input SDTI	LRCK Transition	BICK
0	0	0	0	24-bit, MSB Justified	16-bit, LSB Justified	High to Low	≥32fs
1	0	0	1	24-bit, MSB Justified	20-bit, LSB Justified	High to Low	≥40fs
2	0	1	0	24-bit, MSB Justified	24-bit, MSB Justified	High to Low	≥48fs
3	0	1	1	24-bit, IIS (I^2S)	24-bit, IIS (I^2S)	Low to High[2]	≥48fs
4	1	0	0	24-bit, MSB Justified	24-bit, LSB Justified	High to Low	≥48fs

Notes:

1. Mode 2 is the power-up and reset default mode.
2. Refer to Figure 10.

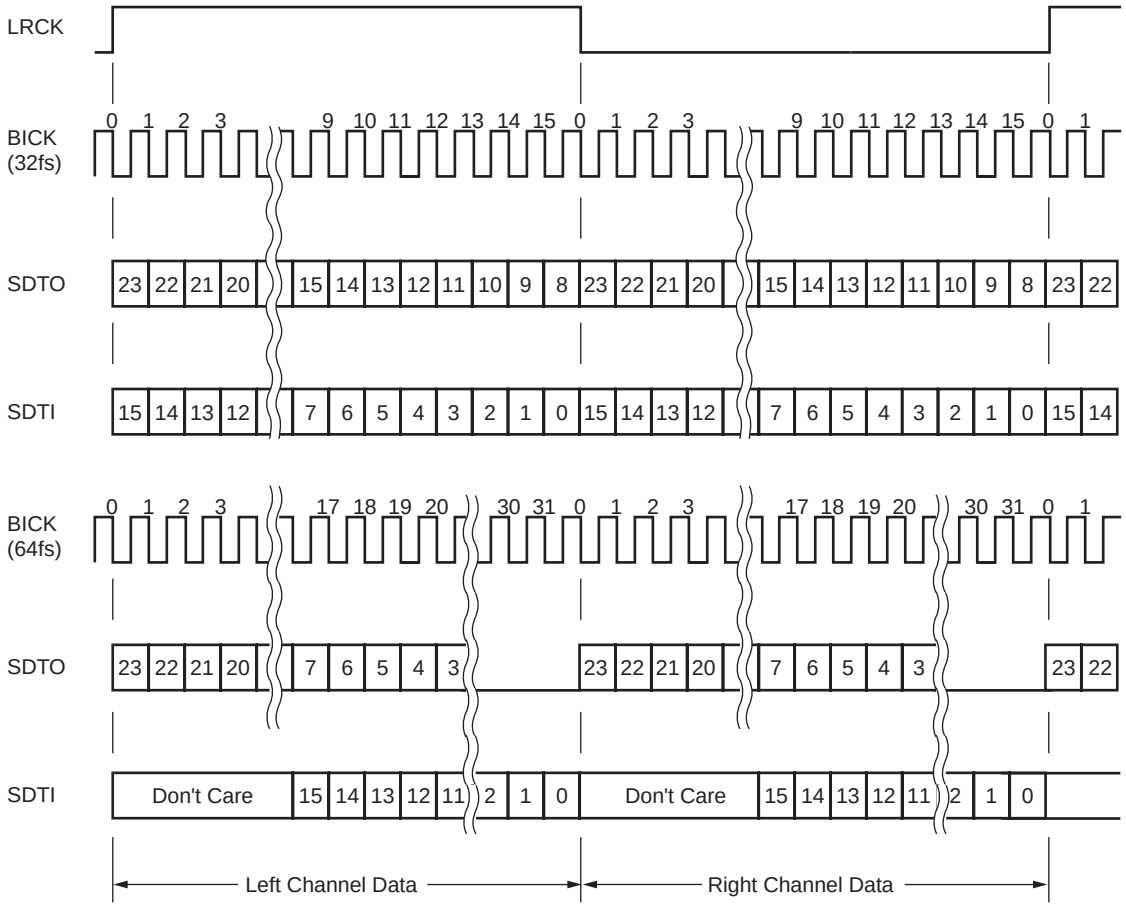


Figure 7. Mode 0 Timing (SDTO: 19 = MSB, 0 = LSB; SDTI: 15 = MSB, 0 = LSB)

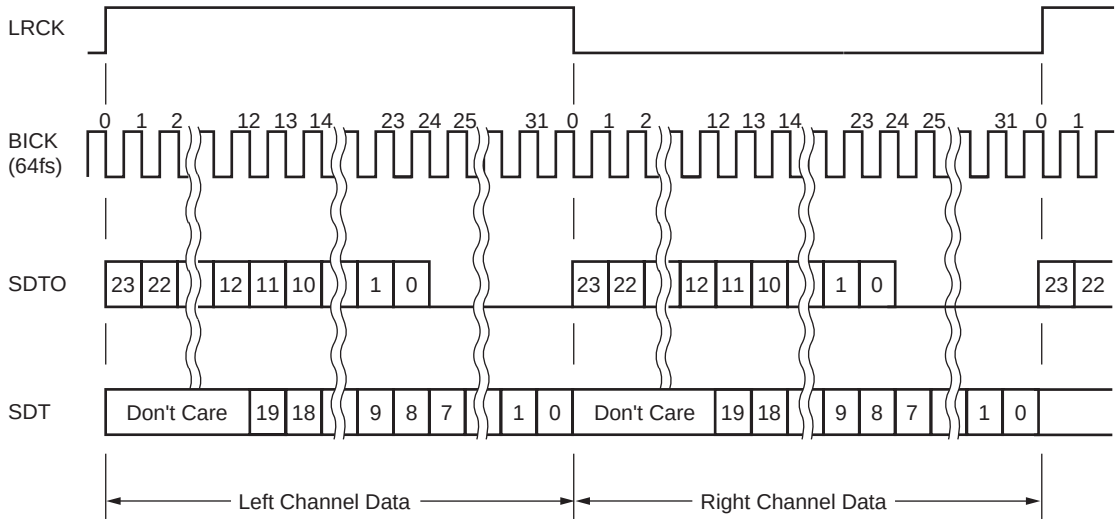


Figure 8. Mode 1 Timing (SDTO: 23 = MSB, 0 = LSB; SDTI: 19 = MSB, 0 = LSB)

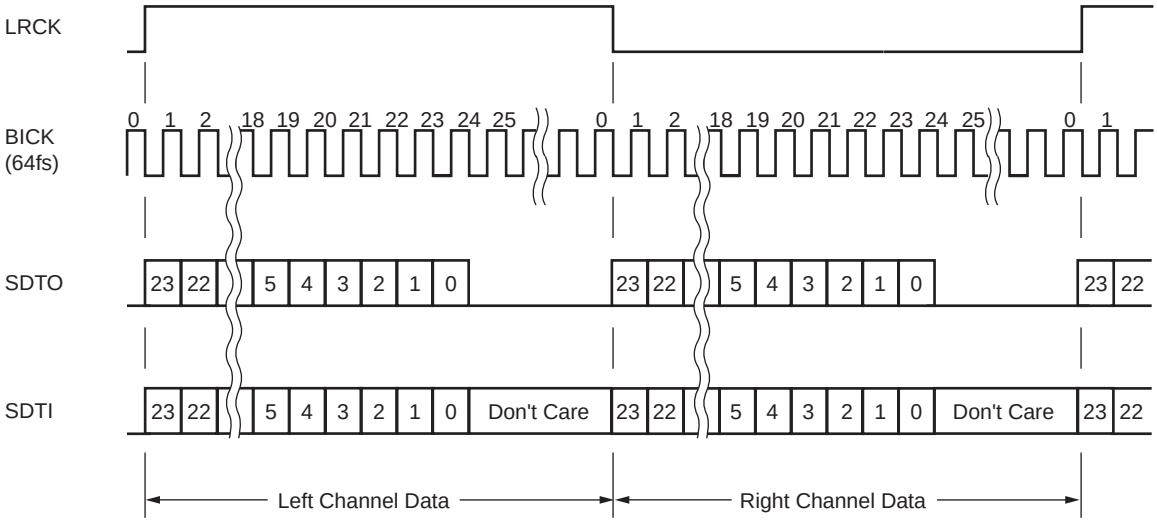


Figure 9. Mode 2 Timing (SDTO and SDTI: 23 = MSB, 0 = LSB)

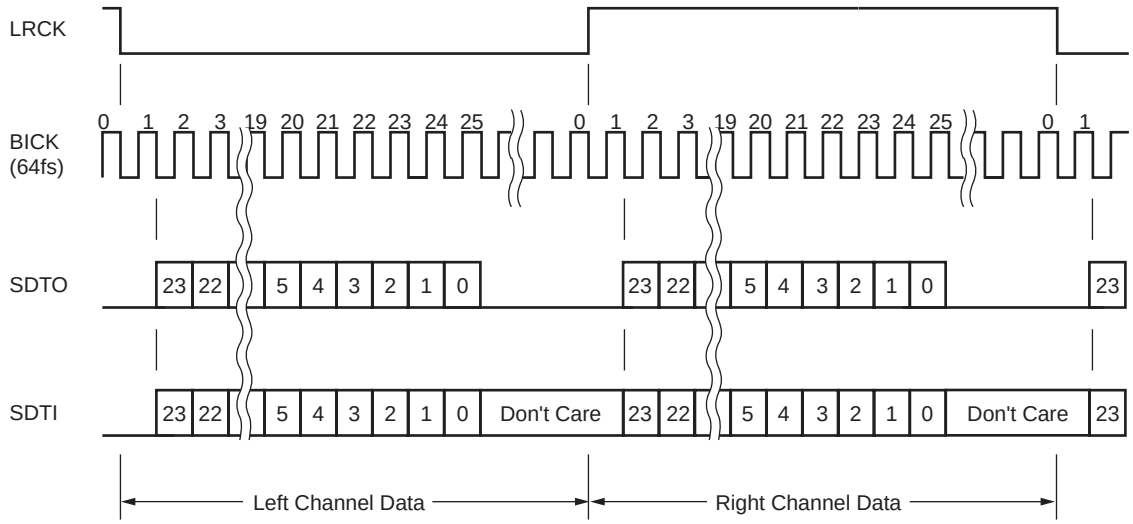


Figure 10. Mode 3 Timing (SDTO and SDTI: 23 = MSB, 0 = LSB)

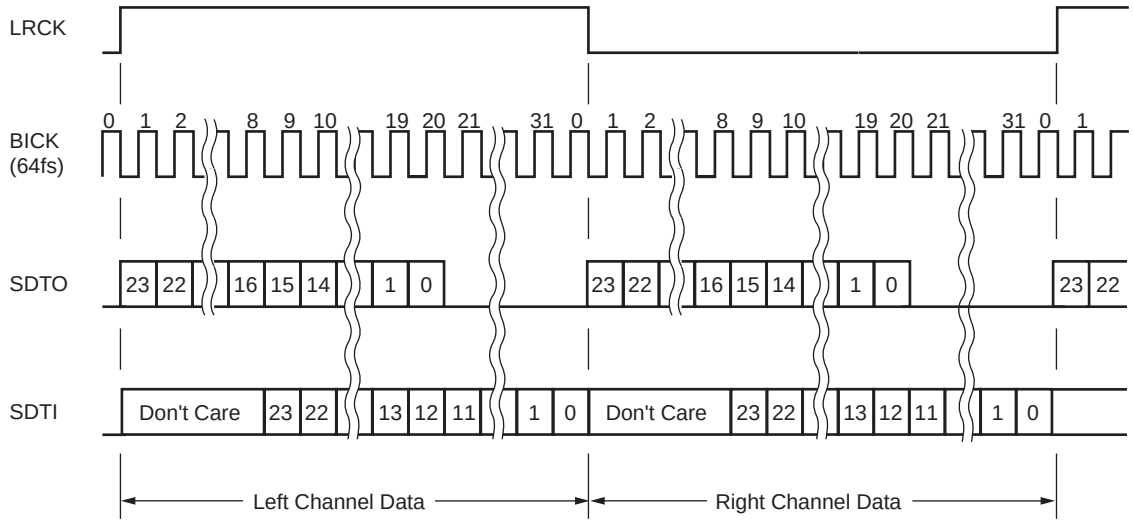


Figure 11. Mode 4 Timing (SDTO and SDTI: 23 = MSB, 0 = LSB)

Input Volume Control

Internally, in front of the ADC, the AK4524 includes two channel-independent programmable gain amplifiers (IPGA) with 37 levels in 0.5dB steps. After the ADC, the AK4524 also includes digital volume controls (IATT) with 128 levels (including MUTE) after the ADC. The control data for these volumes is assigned in the same register address. When programming the part, if the MSB of the control data is 1, the data controls the analog volumes. When the MSB is 0, the data controls the digital volumes (see Table 12).

The two IPGAs improve system signal-to-noise ratio (refer to Table 5) of the ADC. Gain changes only occur at zero-crossings to minimize switching noise. Detection of these crossings is performed independently on each channel. If no zero-crossings occur, then level changes occur after a programmable delay.

Table 5. IPGA + ADC Signal-to-Noise Ratio

Condition	Input Gain Setting		
	0dB	+6dB	+18dB
SNR, fs = 44.1kHz, A-Weighted	100dB	98dB	90dB

The time-out delay period, T0, scales with fs. Delays can be selected using the ZTM1 and ZTM0 bits (refer to Table 6). If a new value is written to an IPGA register before an IPGA change through a zero-crossing or a through a time-out, then the previous IPGA value becomes invalid. At this point, the channel independent timer for time-out delay is reset and restarts for the new IPGA value. The zero-crossing detection can be enabled using the ZCEI bit in the control register.

Table 6. LRCK Cycles for Time-out Delay Periods

ZTM1	ZTM0	fsn	fsd
0	0	256	512
0	1	512	1024
1	0	1024	2048[1]
1	1	2048	4096

Note:

1. The power-on and reset position is ZTM1 = 1 and ZTM0 = 0.

The digital volume control, IATT, uses a pseudo-log volume algorithm for internal linear interpolation, and is composed of 8032 levels. When changing levels, transitions are executed via soft changes; that is, no switching noise occurs during these transitions.

Digital High Pass Filter

The ADC in the AK4524 incorporates a digital high-pass filter (HPF) for DC Offset cancellation. The cut-off frequency for this filter is 0.9Hz at fs = 44.1kHz. This HPF also scales with the sampling rate, fs.

Output Volume

The DAC in the AK4524 includes digital output volume controls (OATT) with 128 levels including MUTE. These controls have the same architecture as the IATTs in front of the DAC. The OATT uses a pseudo-log volume algorithm for internal linear interpolation, and is composed of 8032 levels. When changing levels, transitions are executed via soft changes; that is, no swithching noise occurs during these transitions.

De-emphasis Filter

The DAC in the AK4524 includes a digital de-emphasis filter (tc = 50/15µs) using IIR filtering techniques. This filter can be set for three sampling frequencies (32kHz, 44.1kHz, and 48kHz) and its setting is controlled via registers. See Table 1, Table 7, and Table 11. The filter is always off in the double and the four times speed modes, and at power-on and during reset.

Table 7. De-emphasis Control

Number	DEM1	DEM2	Mode
0	0	0	44.1kHz
1	0	1	Off[1]
2	1	0	48kHz
3	1	1	32kHz

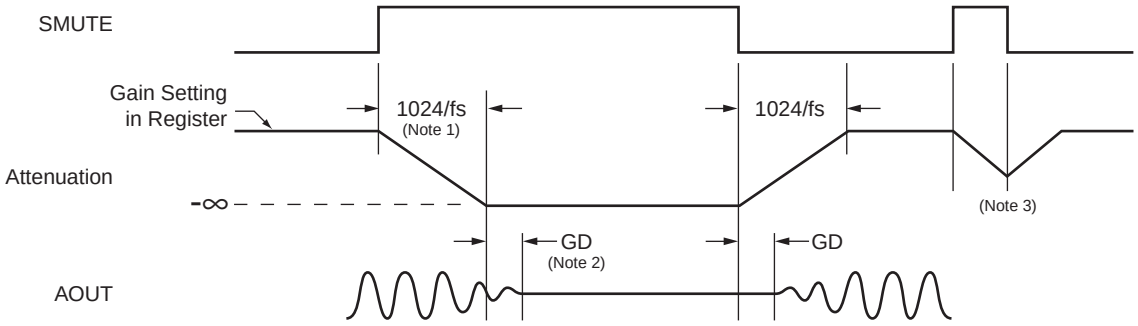
Note:

1. Power-on and reset position.

Soft Mute Operation

The AK4524 can perform a soft mute operation digitally. When SMUTE goes High, the output signal is attenuated to infinity during the next 1024 LRCK cycles. When SMUTE returns to Low, mute is cancelled and the output attenuation gradually changes back, over the next 1024 LRCK clock cycles, to the volume set in the register. If soft mute is cancelled within 1024 cycles after starting the operation, the attenuation is discontinued and volume returns to its previous setting. Soft mute is effective when changing from one signal source to another without stopping signal transmission. Refer to Figure 12.

The soft mute operation is independent of the output volume control and always ramps to infinite attenuation (full scale) over 1024 LRCK clock cycles.



Notes:
1. The output signal is attenuated to -∞ over 1024 cycles (1024/fs).
2. The analog output corresponding to the digital input has a group delay, GD.
3. If soft mute is cancelled within 1024 cycles, attenuation is discontinued and ramps back to the gain selected in the register.

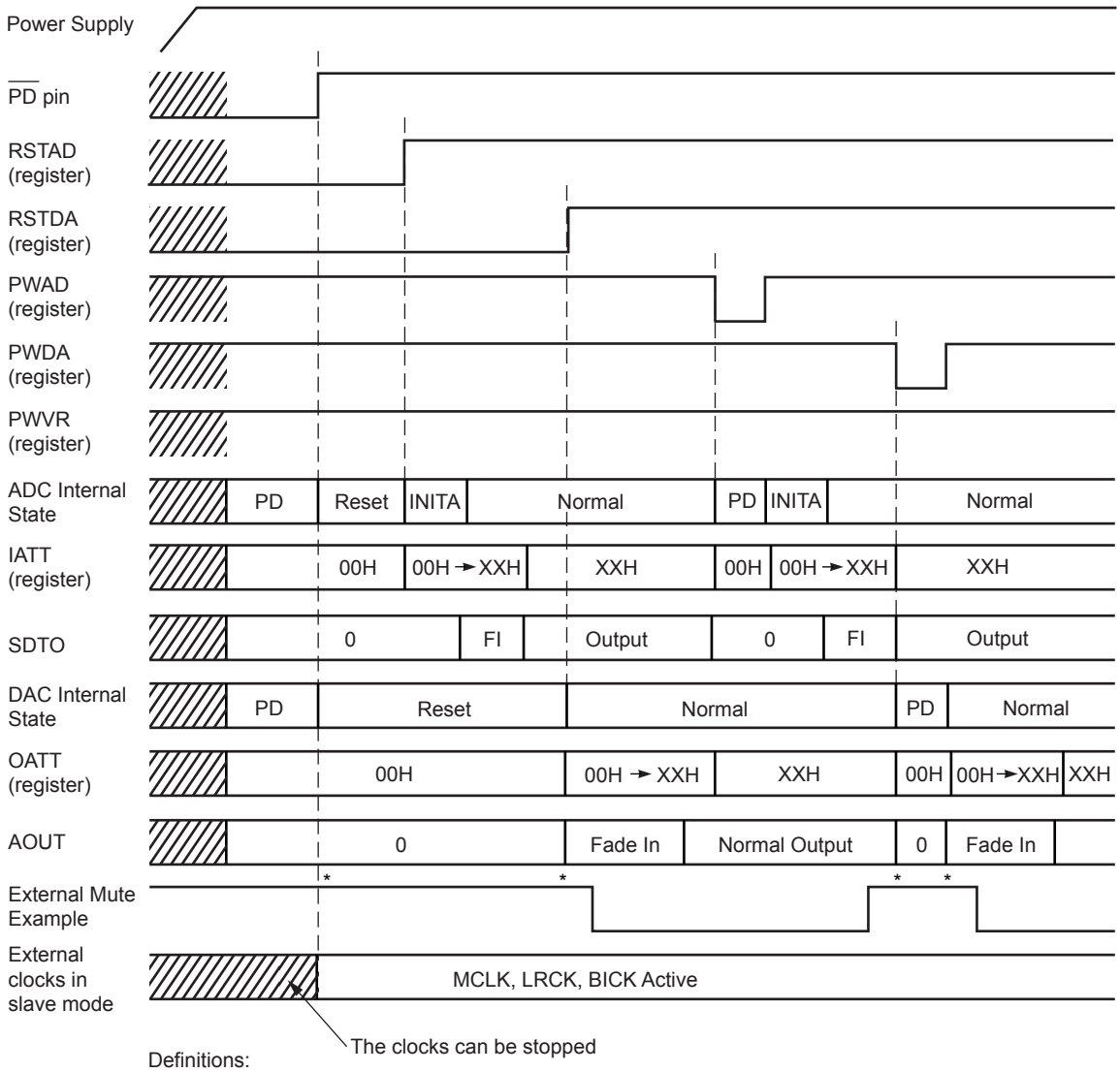
Figure 12. Soft Mute

Power-down and reset

The ADC and DAC of the AK4524 are placed in the power-down mode by setting the $\overline{PD}$ pin Low. During this power-down mode, all digital filters are reset. Thus, to reinitialize the internal register values, set the $\overline{PD}$ pin Low.

After power-up, always reset the registers by taking the $\overline{PD}$ pin to Low. Figure 13 shows the reset and power down sequence. After the reset control registers for the ADC and the DAC go through their reset state (RSTAD = 0 and RSTDA = 0), they should be cancelled by setting them to 1. In the case of the ADC, an analog initialization cycle starts immediately after exiting the power-down or the reset state. Thus, the output data, SDTO, only becomes available after 516 cycles of the LRCK clock. This initialization cycle does not affect the operation of the DAC.

Notice that the power-down mode can also be controlled using the PWAD and PWDA control registers.



Definitions:
INITA: Initializing period of the ADC analog section (516/fs).
PD: Power-down state. The contents of all the registers remain unchanged.
XXH: The current value in the ATT register.
Fade In: After exiting the power-down and reset states, the ATT values ramp to the correct level.
AOUT: Some pop noise may occur where indicated by the asterisks.

Figure 13. Reset and Power-Down Sequence

Relationship Between Clock Operation and Power-Down

The XTALE pin enables or disables the clock signals going into the AK4524. Table 8 shows the XTALE pin operation. When a crystal oscillator is used in master mode, the XTALE pin should be set High. If an external clock is used, then, this pin is set Low.

Table 8. XTALE Pin Operation

Mode	Clock Type	XTALE = L		XTALE = H	
		$\overline{PD}$ = H	$\overline{PD}$ = L	$\overline{PD}$ = H	$\overline{PD}$ = L
Slave M/S = L	Using a Crystal	Inhibit	Inhibit	Normal Operation XTAL = Oscillates CLKO = Output LRCK = Input BICK = Input	Power-down XTAL = Oscillates CLKO = Output LRCK = Input BICK = Input
	Using an External Clock	Normal Operation XTI = MCLK in XTO = L CLKO = L LRCK = Input BICK = Input	Shut Off XTI = MCLK in XTO = L CLKO = L LRCK = Input BICK = Input	Inhibit	Inhibit
Slave M/S = H	Using a Crystal	Inhibit	Inhibit	Normal Operation XTAL = Oscillates CLKO = Output LRCK = Output BICK = Output	Power-down XTAL = Oscillates CLKO = Output LRCK = H BICK = L
	Using an External Clock	Normal Operation XTI = MCLK in XTO = L CLKO = L LRCK = Output BICK = Output	Shut Off XTI = MCLK in XTO = L CLKO = L LRCK = H BICK = L		

Control Register Setup Sequence

After power on, the AK4524 should be brought into operation as follows:

1. Keep $\overline{PD}$ low while the supply stabilize.
2. After supplies are stable, set $\overline{PD}$ High. All the AK4524 regulators go to their default values.
3. Set the clock mode and the audio data interface mode.
4. Cancel the reset state by setting RSTAD or RSTDA to 1. Refer to Control Register Definitions section.
5. The ADC outputs and DAC outputs should be muted externally until each reset state is cancelled. In the master mode, the possibility exists that the frequency and duty cycle of the LRCK and BICK outputs may go into an abnormal state.

The clock mode should be changed after setting RSTAD and RSTDA to 0; then, the ADC and DAC outputs should be muted externally. In the master mode, the possibility exists that the frequency and duty cycle of the LRCK and BICK outputs may go into an abnormal state.

Mode Control Interface

The internal registers may be written to using the three micro-controller interface pins: CS, CCLK, and CDTI. The data on this interface consists of a 2-bit chip address (C0 and C1), a 1-bit read/write bit, a 5-bit register address (in MSB-first format), and 8 bits of control data (in MSB-first format). The AK4524 clocks this data on the rising edge of CCLK, and the data is latched after the sixteenth rising edge and after the high-to-low transition of CS. Refer to Figure 14.

The operation of the control serial port may be completely asynchronous with the audio sample rate. The maximum clock speed of CCLK is 5MHz. The CS pin can be set High or Low as its trigger is determined by the input to the CIF pin, which occurs when the chip addess is fixed to 10. Thus, writing to the chip is only possible when the chip address is 10. Setting the $\overline{PD}$ pin Low resets all registers to their default values.

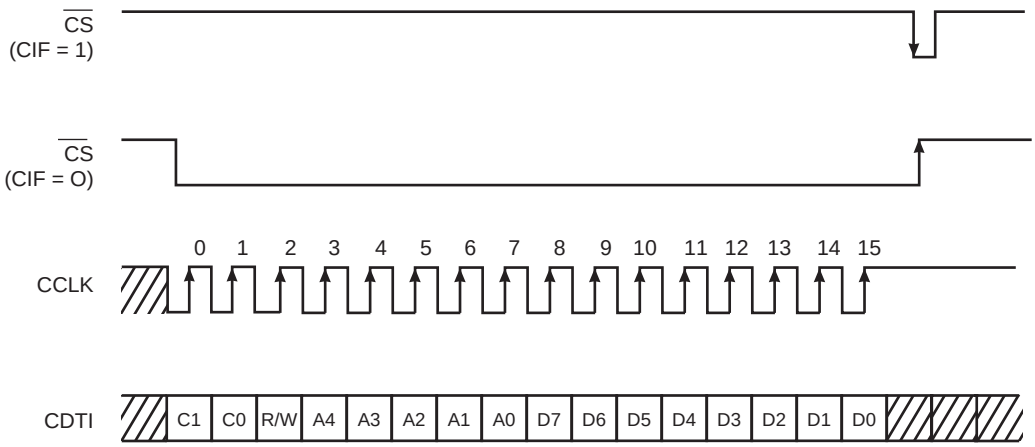


Figure 14. Control Interface Timing

Register Map

Table 10 shows the register map for the AK4524.

Table 10. Register Map

Address Name	Control Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Default & Reset
00H	Power Down	0	0	0	0	0	PWVR	PWAD	PWDA	00000111
01H	Reset	0	0	0	0	0	0	RSTAD	RSTDA	00000000
02H	Clock and Format	DIF2	DIF1	DIF0	CMODE	CKS1	CKS0	DFS1	DFS0	01000000
03H	Deem and Volume	SMUTE	0	0	ZCEI	ZTM1	ZTM0	DEM1	DEM0	00011001
04H	Left Channel IPGA	IPGL7	IPGL6	IPGL5	IPGL4	IPGL3	IPGL2	IPGL1	IPGL0	01111111
05H	Right Channel IPGA	IPGR7	IPGR6	IPGR5	IPGR4	IPGR3	IPGR2	IPGR1	IPGR0	01111111
06H	Left Channel ATT	0	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0	01111111
07H	Right Channel ATT	0	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0	01111111

Notes:

1. Data cannot be written to addresses 08H to 1FH.
2. Setting the $\overline{PD}$ pin to Low resets the registers to their default values.

Control Register Definitions

Table 11 expands the register map on the previous section and shows the function for each bit in each register. Notice that the reset values are included. Setting the $\overline{PD}$ pin Low resets the registers to their default values.

Table 11. Control Register Definitions

Bit(s)	Bit Name	Reset Value	Function
Power Down Control Register: Address 00H			
D7 - D3	0	0	**Not Defined**
D2	PWVR	1	**VREF Power-down** • When the PWVR bit is set to 1, the ADC and DAC are both powered up. • When the PWVR bit is set to 0, the ADC and DAC are both powered down. The registers are not initialized and can accept new data. When the PWAD and PWDA bits are both zero, then only the VREF section is powered.
D1	PWAD	1	**ADC Power-down** • When the PWAD bit is set to 1, the ADC is powered up. • When the PWAD bit is set to 0, the ADC is powered down, and the SDTO bit goes Low. The IPGAs are also reset when this bit is zero. In addition, since the registers are not initialized, they maintain the old data and can accept new data. After exiting the power-down mode, the IPGAs ramp to the values set in registers 04H and 05H.
D0	PWDA	1	**DAC Power-down** • When the PWDA bit is set to 1, the DAC is powered up. • When the PWDA bit is set to 0, the DAC is powered down, and the AOUT+ and AOUT- pins go to Hi-Z immediately. The OATTs are also reset when this bit is set to 0, and since all the registers are not initialized, they maintain the old data and can accept new data. After exiting the power-down mode, the OATTs fade to the values set in registes 06H and 07H. The extenal output amplifiers should be muted externally to avoid pop noises occurring when entering and exiting this mode.
Reset Control Register: Address 01H			
D7 - D2	0	0	**Not Implemented.** Do not write to these bits.
D1	RSTAD	0	**ADC Reset** • When the RSTAD bit is set to 1, the ADC is in normal operation. • When the RSTAD bit is set to 0, the internal timing of the ADC is reset, and the SDTO pin goes Low. In addition, the IPGAs are reset when this bit is 0, and since all registers are not initialized, they maintain the old data and can accept new data. After exiting the power-down mode, the IPGAs ramp to the values set in registers 04H and 05H.
D0	RSTDA	0	**DAC Reset** • When the RSTDA bit is set to 1, the DAC is in normal operation. • When the RSTDA bit is set to 0, the timing of the DAC is reset, and the AOUT+ and AOUT- pins immediately jump to the VCOM voltage. In addition, the OATTs are reset when this bit is set to 0, and since all the registers are not initialized, they can accept new data. After exiting the power-down mode, the OATTs ramp to the values set in registes 06H and 07H. The external output amplifiers should be muted externally to avoid pop noises occurring when entering and exiting this mode.
Clock and Format Control Register: Address 02H			
D7	DIF2	0	**Audio Data Interface Modes** See Table 4. Default values are for 24-bit MSB justified data formats for both ADC and DAC.
D6	DIF1	1	
D5	DIF0	0	
D4	CMODE	0	**Master Clock Frequency Select** See Table 1 for functions. Default value is 256fs.
D3	CKS1	0	
D2	CKS0	0	
D1	DFS1	0	**Sampling Speed Control** See Table 2 for functions. Default value is normal speed.
D0	DFS0	0	

Bit(s)	Bit Name	Reset Value	Function
De-emphasis and Volume Control: Address 03H			
D7	SMUTE	0	**DAC Input Soft Mute Control** When the SMUTE bit is set to 1, the output signal is attenuated to infinity during the next 1024 LRCK cycles. When this bit is set to 0, the mute is cancelled and the output attenuation gradually returns to the volume setting in the register. The soft mute is performed digitally and independent of the digital volumes, OATT.
D6 - D5	0	0	**Not Implemented.** Do not write to these bits.
D4	ZCEI	1	**ADC IPGA Zero Crossing Enable** When the ZCEI bit is set to 1, then IPGA gain changes occur immediately. When this pin is set to 0, then IPGA gain changes occur only at zero-crossings or after time-outs when they are written to the registers.
D3	ZTM1	1	**Zero Crossing Time Out Period Select** See Table 6. The default value is 1024fs.
D2	ZTM0	0	
D1	DEM1	0	**De-emphasis Response** See Table 7. The default is No De-emphasis.
D0	DEM0	1	
ADC Input Gain Level—Left Channel IPGA Control Register: Address 04H			
D7	IPGL7	0	**Left Channel IPGA Control** See Table 12. The default value is 7FH or 0dB. The digital ATT is active when data of less than 7FH is written. This linear digital ATT has 8032 internal levels in a pseudo-log distribution that yield 128 external levels. Transitions between levels occur via soft changes. For example, an external change from 127 to 126 is equivalent to an internal transition between 8031 and 7775; each step takes one fs cycle. It takes 8031 cycles (182ms at fs = 44.1kHz) to transiton from 127 (full scale) to 0 (mute). The IPGAs are 00H when the PD pin is Low. When PD is switched to High, the IPGAs fade from the initial value, 7FH, through 8031 cycles. The IPGAs are 00H when the PWAD or when the RSTAD is 0. When these registers return to 1, the IPGAs ramp to their current value, but the ADCs output 0 for the first 516 cycles.
D6	IPGL6	1	
D5	IPGL5	1	
D4	IPGL4	1	
D3	IPGL3	1	
D2	IPGL2	1	
D1	IPGL1	1	
D0	IPGL0	1	
ADC Input Gain Level—Right Channel IPGA Control Register: Address 05H			
D7	IPGR7	0	**Right Channel IPGA Control** See Table 12. Initial value is 7FH or 0dB. The digital ATT is active when data of less than 7FH is written. This linear digital ATT has 8032 internal levels in a pseudo-log distribution that yield 128 external levels. Transitions between levels occur via soft changes. For example, an external change from 127 to 126 is equivalent to an internal transition between 8031 and 7775; each step takes one fs cycle. It takes 8031 cycles (182ms at fs = 44.1kHz) to transiton from 127 (full scale) to 0 (mute). The IPGAs are 00H when the PD pin is Low. When PD is switched to High, the IPGAs fade from the initial value, 7FH, through 8031 cycles. The IPGAs are 00H when the PWAD or when the RSTAD is 0. When these registers return to 1, the IPGAs fade to their current value, but the ADCs output 0 for the first 516 cycles.
D6	IPGR6	1	
D5	IPGR5	1	
D4	IPGR4	1	
D3	IPGR3	1	
D2	IPGR2	1	
D1	IPGR1	1	
D0	IPGR0	1	
DAC Output ATT Level—Left Channel OATT Control Register: Address 06H			
D7	0	0	**Left OATT Control** See Table 13. Initial value is 7FH or 0dB. The digital ATT is active when data of less than 7FH is written. This linear digital ATT has 8032 internal levels in a pseudo-log distribution that yield 128 external levels. Transitions between levels occur via soft changes. For example, an external change from 127 to 126 is equivalent to an internal transition between 8031 and 7775; each step takes one fs cycle. It takes 8031 cycles (182ms at fs = 44.1kHz) to transiton from 127 (full scale) to 0 (mute). The OATTs are 00H when the PD pin is Low. When PD is switched to High, the OATTs fade from the initial value, 7FH, through 8031 cycles. The OATTs are 00H when the PWAD or when the RSTAD is 0. When these registers return to 1, the OATTs fade to their current value.
D6	ATTL6	1	
D5	ATTL5	1	
D4	ATTL4	1	
D3	ATTL3	1	
D2	ATTL2	1	
D1	ATTL1	1	
D0	ATTL0	1	

Bit(s)	Bit Name	Reset Value	Function
DAC Output ATT Level—Left Channel OATT Control Register: Address 06H			
D7	0	0	**Left OATT Control** See Table 13. Initial value is 7FH or 0dB. The digital ATT is active when data of less than 7FH is written. This linear digital ATT has 8032 internal levels in a pseudo-log distribution that yield 128 external levels. Transitions between levels occur via soft changes. For example, an external change from 127 to 126 is equivalent to an internal transition between 8031 and 7775; each step takes one fs cycle. It takes 8031 cycles (182ms at fs = 44.1kHz) to transiton from 127 (full scale) to 0 (mute). The OATTs are 00H when the PD pin is Low. When PD is switched to High, the OATTs fade from the initial value, 7FH, through 8031 cycles. The OATTs are 00H when the PWAD or when the RSTAD is 0. When these registers return to 1, the OATTs fade to their current value.
D6	ATTR6	1	
D5	ATTR5	1	
D4	ATTR4	1	
D3	ATTR3	1	
D2	ATTR2	1	
D1	ATTR1	1	
D0	ATTR0	1	

Table 12. IPGA Code Table (Addresses 04H and 05H)

Data	Internal Level	Gain (dB)	Step Size (dB)	Comments
255 - 165	-	+18	-	**IPGA** Analog volume with 0.5dB steps.
164	-	+18	-	
163	-	+17.5	0.5	
162	-	+17	0.5	
. . .	-	. . .	0.5	
130	-	+1.0	0.5	
129	-	+0.5	0.5	
128	-	0	0.5	
127	8031	0	-	**IATT** The 128 external levels are converted into the 8032 internal linear levels of a Digital ATT (DATT). ATT soft-changes when transitions between data occur. DATT = $2^m(2l + 33) - 33$ Where, m is the MSB of the 3-bit data, and l is the LSB of the 4-bit data.
126	7775	-0.28	0.28	
125	7519	-0.57	0.29	
. . .	-	. . .	. . .	
112	4191	-5.65	0.51	
111	3999	-6.06	0.41	
110	3871	-6.34	0.28	

Data	Internal Level	Gain (dB)	Step Size (dB)	Comments
. . .	-	. . .	. . .	**IATT** The 128 external levels are converted into the 8032 internal linear levels of a Digital ATT (DATT). Then internal digital ATT soft-changes when transitions between data occur. DATT = $2^m(2l + 33) - 33$ Where, m is the MSB of the 3-bit data, and l is the LSB of the 4-bit data.
96	2079	-11.74	0.52	
95	1983	-12.15	0.41	
94	1919	-12.43	0.28	
. . .	-	. . .	. . .	
79	1023	-17.90	0.53	
78	975	-18.32	0.42	
77	943	-18.61	0.29	
. . .	-	. . .	. . .	
64	495	-24.20	0.54	
63	471	-24.64	0.43	
62	455	-24.94	0.30	
. . .	-	. . .	. . .	
48	231	-30.82	0.58	
47	219	-31.29	0.46	
46	211	-31.61	0.32	
. . .	-	. . .	. . .	
32	99	-38.18	0.67	
31	93	-38.73	0.54	
30	89	-39.11	0.38	
. . .	-	. . .	. . .	
16	33	-47.73	0.99	
15	30	-48.55	0.83	
14	28	-49.15	0.60	
. . .	-	. . .	. . .	
5	10	-58.10	1.58	
4	8	-60.03	1.94	
3	6	-62.53	2.50	
2	4	-66.05	3.52	
1	2	-72.07	6.02	
0	0	MUTE		

Table 13. OATT Code Table

Data	Internal Level	Gain (dB)	Step Width (dB)	Comments
127	8031	0	-	**OATT** The 128 external levels are converted into the 8032 internal linear levels of a Digital ATT (DATT). Then internal digital ATT soft-changes when transitions between data occur. DATT = $2^m(2l + 33) - 33$ Where, m is the MSB of the 3-bit data, and l is the LSB of the 4-bit data.
126	7775	-0.28	0.28	
125	7519	-0.57	0.29	
. . .	-	. . .	. . .	
112	4191	-5.65	0.51	
111	3999	-6.06	0.41	
110	3871	-6.34	0.28	
. . .	-	. . .	. . .	
96	2079	-11.74	0.52	
95	1983	-12.15	0.41	
94	1919	-12.43	0.28	
. . .	-	. . .	. . .	
79	1023	-17.90	0.53	
78	975	-18.32	0.42	
77	943	-18.61	0.29	
. . .	-	. . .	. . .	
64	495	-24.20	0.54	
63	471	-24.64	0.43	
62	455	-24.94	0.30	
. . .	-	. . .	. . .	
48	231	-30.82	0.58	
47	219	-31.29	0.46	
46	211	-31.61	0.32	
. . .	-	. . .	. . .	
32	99	-38.18	0.67	
31	93	-38.73	0.54	
30	89	-39.11	0.38	
. . .	-	. . .	. . .	
16	33	-47.73	0.99	
15	30	-48.55	0.83	
14	28	-49.15	0.60	

Data	Internal Level	Gain (dB)	Step Width (dB)	Comments
. . .	-	. . .	. . .	**OATT** The 128 external levels are converted into the 8032 internal linear levels of a Digital ATT (DATT). Then internal digital ATT soft-changes when transitions between data occur. DATT = $2^m(2l + 33) - 33$ Where, m is the MSB of the 3-bit data, and l is the LSB of the 4-bit data.
5	10	-58.10	1.58	
4	8	-60.03	1.94	
3	6	-62.53	2.50	
2	4	-66.05	3.52	
1	2	-72.07	6.02	
0	0	MUTE		

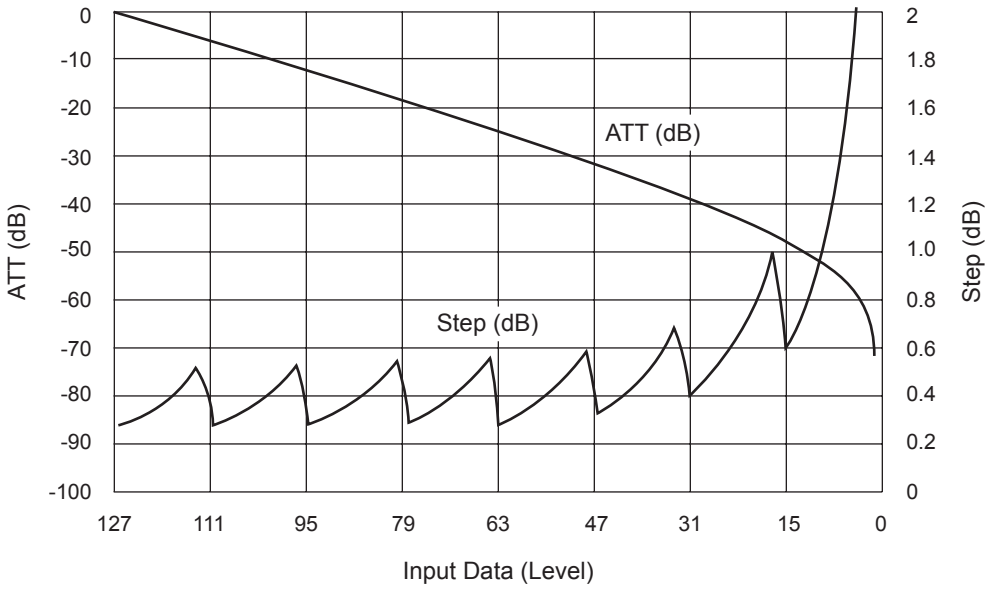
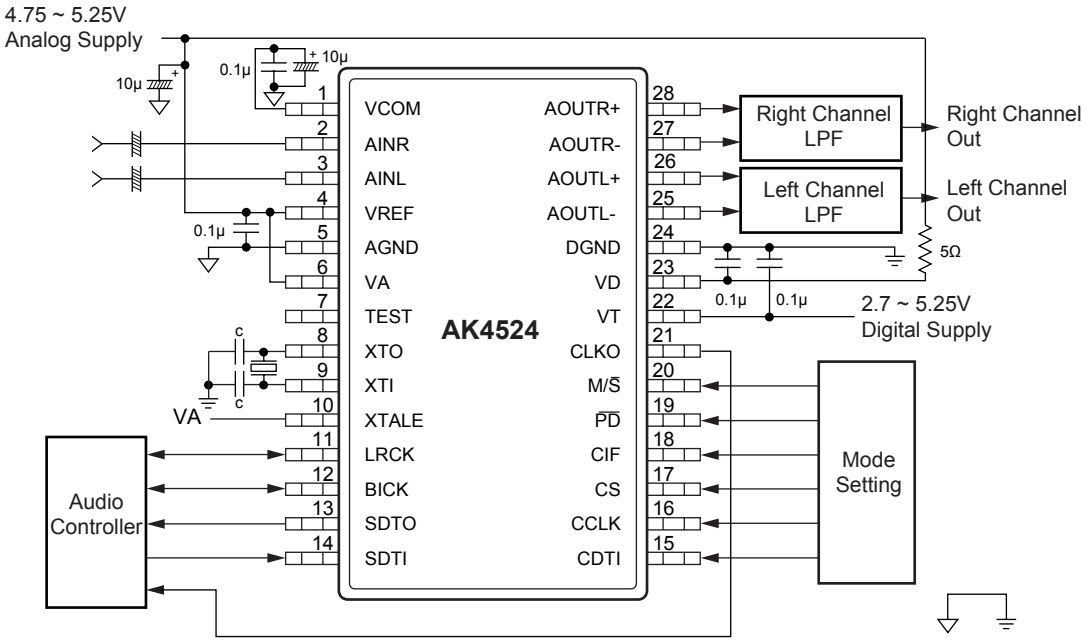


Figure 15. ATT Characteristics

Design Considerations

Figure 16 shows a connection diagram for the AK4524 when using a crystal oscillator. Figure 17 show a system connection diagram for the AK4524 when using an external clock. An evaluation board for this device is available to demonstrate the applications circuits, an optimum layout, power supply arrangements, and measuring results—see the Ordering Information section. Table 14 shows various external capacitances required between the crystal oscillator and ground (see Figure 16).



Notes:

- The crystal oscillator circuit is specified from 11.2892MHz to 24.576MHz.
- The AGND and DGND pins should be kept separate from the grounds used primarily by digital components, such as the controller.
- When the AOUT+ and AOUT- pins drive some capacitive load, resistors should be added in series between these pins and the capacitive load.
- All input pins (except the TEST pin) should be connected.

Figure 16. Typical Connection Diagram for Crystal Mode

Table 14. Example of External Capacitors when Using a Crystal Oscillator

Crystal Frequency	C
11.2896MHz and 12.288MHz	33pF
16.384MHz, 16.9344MHz, and 18.432MHz	15pF
22.5792MHz and 24.576MHz	10pF

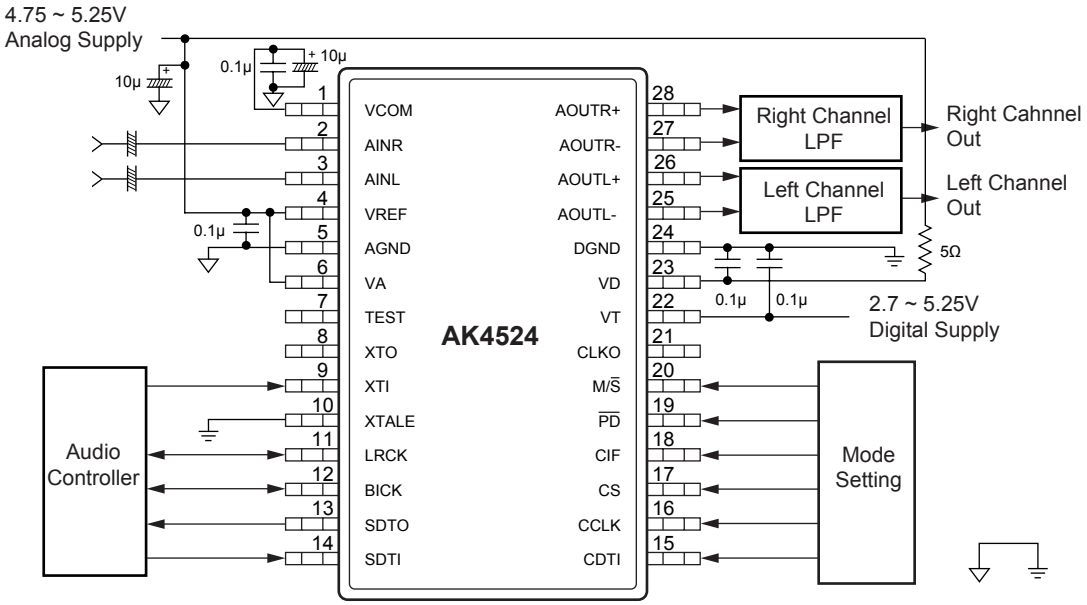


Figure 17. Typical Connection Diagram for External Clock Mode

Grounding and Power Supply Decoupling

Careful attention should be observed for the power supply and grounding of the AK4524. **VA and VD are normally supplied from the analog supply in the system.** Optimum performance in most systems is achieved by using one power supply for both VA and VD.

If VA and VD are supplied separately, care should be taken as follows:

- The VT power supply pin, used to interface with other devices in the circuit, must be supplied from the system's digital power supply.
- VT is the digital I/O power supply and must be applied before any logig inputs or outputs are transitioned.
- The systems analog and digital grounds should be connected together close to where the supplies are brought together into the printed circuit board.
- The decoupling capacitors should be as close to the AK4524 as possible, with the smaller valued ceramic capacitor being the one nearest to the CODEC.

Voltage Reference

The differential voltage between VREF and AGND determines the input/output range. The VREF pin is normally connected to VA with a 0.1µF ceramic capacitor. VCOM is the AK4524's signal ground. A 10µF eletrolytic capacitor in parallel with a 0.1µF ceramic capacitor, and connected to the VCOM pin eliminates the effects of high frequency noise. No load current should be drawn from the VCOM pin. All signals, especially clock signals, should be kept away from the VREF and the VCOM pins to avoid unwanted signal coupling going into the AK4524.

Analog Inputs

The IPGA inputs are single-ended with a minimum input resistance of 5kΩ. The input signal range is proportional to the VREF voltage and is 0.58VREF V_{P-P} nominally. The AK4524 can accept input voltages from the AGND pin to the VA pin. Using VA provides the widest signal dynamic range.

The ADC output data format is 2's Complement formatted. For 24-bit data, the output code is 7FFFFFH for input above a positive full scale and 800000H for input below a negative full scale. The ideal code for 24-bit data is 000000H with no input signal. Any DC offset is removed by the internal HPF.

The AK4524 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for all multiples of 64fs. The device also includes an anti-aliasing (RC) filter to attenuate the noise around 64fs; thus minimal external anti-aliasing filters are required.

Analog Outputs

The analog outputs are full differential outputs and normally 0.54 x VREF V_{P-P} centered around VA/2. The differential outputs are summed externally between AOUT+ and AOUT-: VAOUT = (AOUT+) - (AOUT-). If the summing gain is 1, then the output range is $5.4V_{P-P}$ (typical at VREF = 5V). The bias voltage for the external summing circuit should be supplied externally.

The input data is 2's complement formatted. For 24-bit data, the output voltage (VAOUT) is a positive full scale for 7FFFFFH and a negative full scale for 800000H. The ideal VAOUT for 24-bit data is 000000H.

The internal switched-capacitor filter and the external LPF attenuate the noise generated by the ΔΣ modulator above the audio passband.

The DC offset on analog outputs is eliminated by AC coupling since the differential outputs have a DC offset of VA/2 plus a few millivolts. Figures 18, 19, and 20 show external op-amp circuits summing the differential outputs.

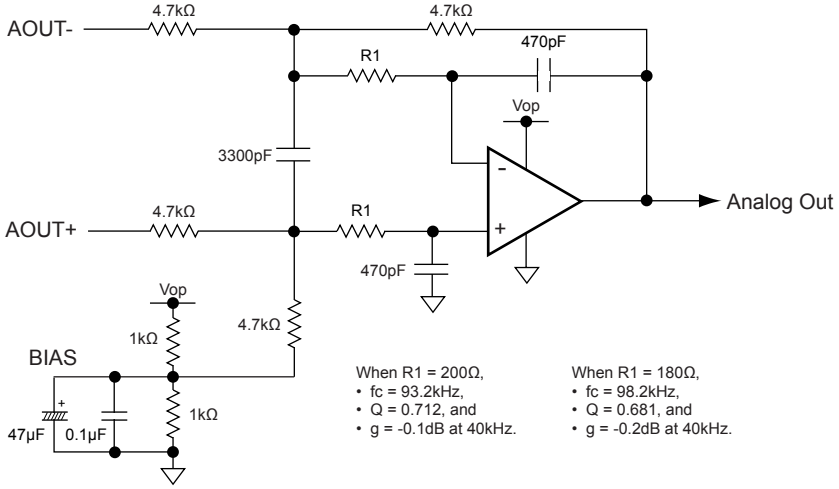


Figure 18. External 2nd Order LPF Circuit Example (Using a Single Supply Op-Amp)

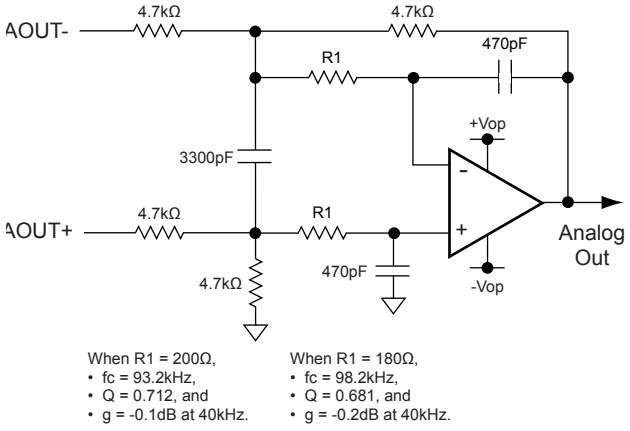


Figure 19. External 2nd Order LPF Example (Using a Dual Supply Op-Amp)

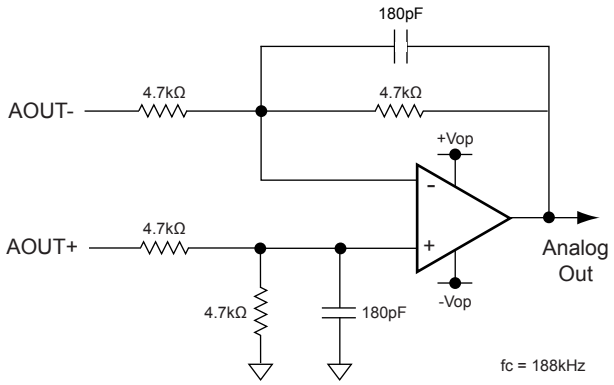


Figure 20. External Low-Cost 1st Order LPF Example (Using a Dual Supply Op-Amp)

Peripheral Interface Example

The digital inputs of the AK4524 are TTL and can interface to devices with either 5V or 3.3V logic supplies. When the VT supply operates at a nominal 3.3V supply, the AK4524 can interface with peripheral devices that have nominal 3.3V supplies. Figure 21 shows a power supply connection circuit.

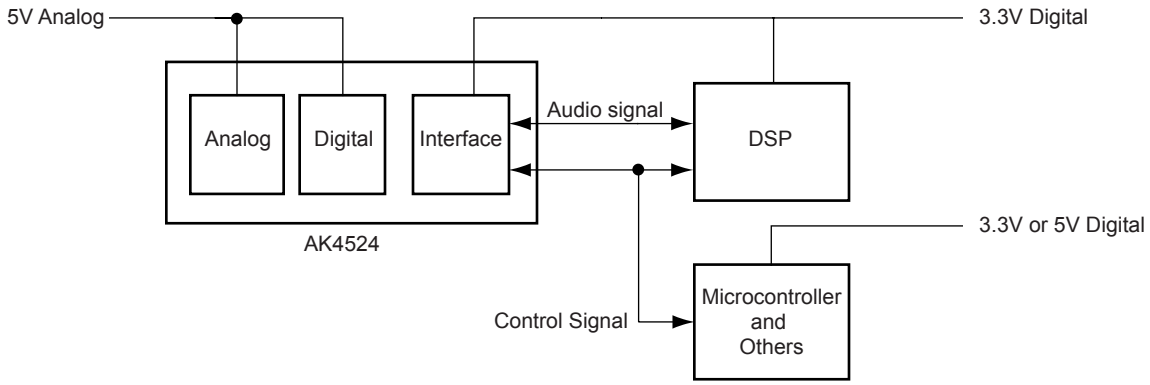


Figure 21. Power Supply Connection Example

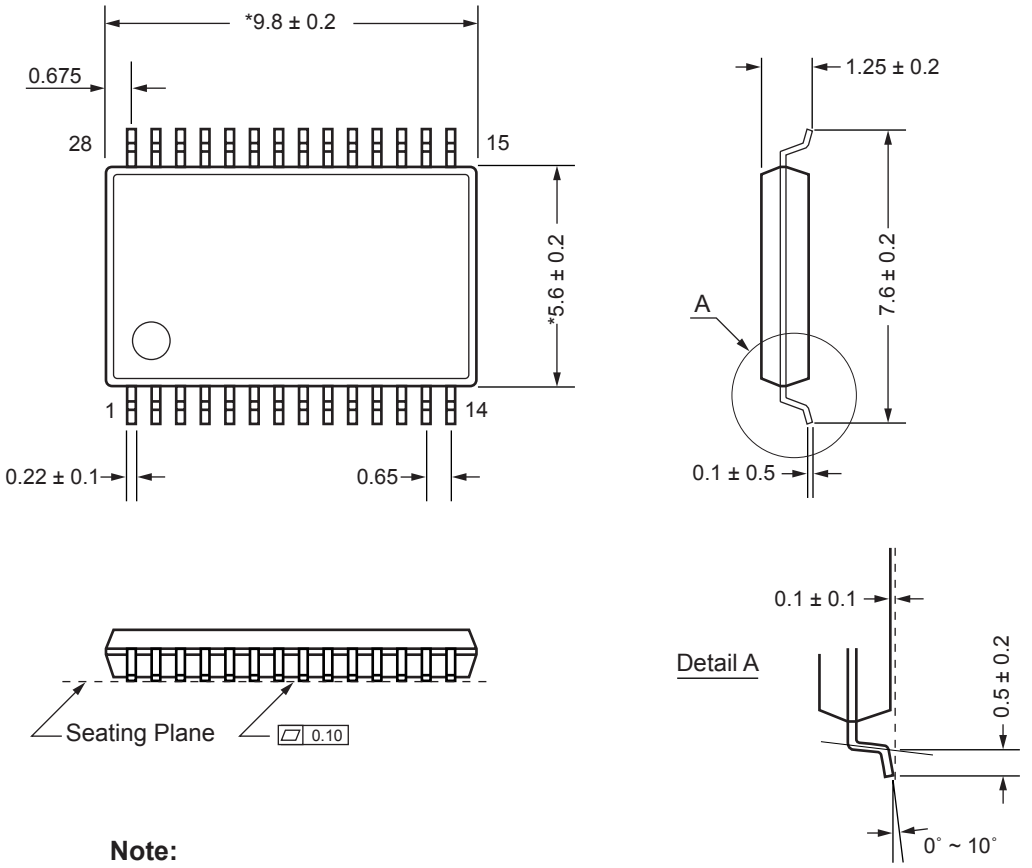
Notes:

Notes:

Package Dimensions

28 Pin VSOP

Units: mm

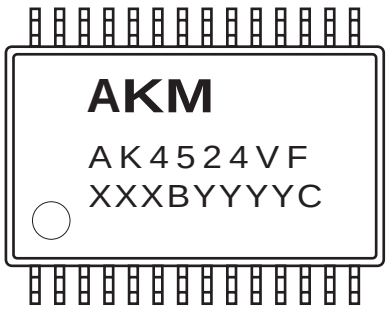


Note:
1. Dimension labeled with an asterisk (*) do not include mold flash.

Material and Lead Finish:

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder Plate

Package Markings



XXXBYYYYC: Data Code Identifier

XXXB: Lot Number (X: Digit Number, B: Alpha Character)
YYYYC: Assembly Date (YYYY: Digit Number, C: Alpha Character)

Ordering Information

Part Number	Temperature Range	Package
AK4524VF	-10˚C to +70˚C	28 Pin VSOP (0.65mm Pitch)
AKD4524		Evaluation Board